REMARKS

Applicant has carefully reviewed the comments, objections, and rejections set forth by the Examiner in the Office Action dated April 26, 2004 and respectfully respond with the amendments above and the following remarks. Claims 1-3, 5, 7-12, and 14-21 are pending in the present case. Claim 5 is cancelled herein. (Claims 4, 6, and 13 are cancelled in previous correspondence.) Claims 1, 11, 14, and 20 are amended herein. Applicant respectfully requests reconsideration in view of the above amendments and the arguments set forth below.

ALLOWABLE SUBJECT MATTER

The Applicant respectfully thanks the Examiner for pointing out that Claims 5, 8, 10-12, and 15-19 contain allowable subject matter. Claim 5 is cancelled herein. Independent Claim 1 is amended herein to incorporate the allowable subject matter of Claim 5. Claims 14 and 20 are amended herein to comport with statute.

REJECTIONS UNDER 35 USC 112

In the Office Action, Claims 14-21 are rejected under 35 USC 112 (second paragraph). Claims 14 and 21 were deemed misdescriptive, for reciting "which causes a capacitor to switch between ground and a node". As amended herein, Claims 14 and 21 read as follows:

> 14. A switched capacitor controller for controlling a rise time of an on-chip generated voltage source, comprising:
>
> a charge pump;

a ramp generator coupled to said charge pump, wherein said ramp generator comprises a switched capacitor;

a regulator circuit coupled to said switched capacitor circuit which causes a capacitor to switch between ground potential and the potential at a node, wherein a stair-step ramp signal is generated and said rise time is controlled with said switched capacitor.

21. The method of Claim 20 further comprising switching a capacitor between ground potential and the potential at a node to generate said stair-case ramp.

(underlining added herein for emphasis). As amended herein, Claims 14 and 21 recite that the capacitor is caused to switch between ground potential and the potential at a node (element 136; Fig. 1 of the specification).

Applicant respectfully asserts that, as amended herein to delineate that the potentials between which the capacitor is switched are that of ground and that at the node, Claims 14 and 21 comport with 35 USC 112 (second paragraph).

Claim 20 was rejected as misdescriptive because the clock signal recited in the claim was not clear from the drawings. As amended herein, Claim 20 reads as follows:

20. In a flash memory, a method for controlling a rise time of an on-chip generated voltage source used to program said flash memory, comprising:

generating a programming voltage VPP from a power supply, wherein said programming voltage is greater than a supply voltage VCC from said power supply;

activating a program control signal ENVPP to enable programming a cell of said flash memory;

generating a stair-case ramp based on said programming voltage VPP in response to said program control signal ENVPP, wherein steps of said stair-case ramp have a period corresponding to a clock signal generated by a clock generator and voltage increases corresponding to a reference voltage times a ratio of two capacitor values.

(underlining added herein for emphasis). As amended herein, Claim 20 recites that the programming voltage VPP, which is greater than supply voltage VCC, is generated by a power supply, clarifies the program enabling signal in the "activating" step as the program control signal ENVPP, and generates the stair case ramp based on the programming voltage VPP in response to the control signal ENVPP. These voltage and signal designations and the method recited in Claim 20 is explained in detail in the specification generally from line 14 at page 6 to line 24 at page 11 (and elsewhere), and somewhat more particularly from line 1 at page 7 through line 6 at page 11.

Applicant respectfully asserts that, as amended herein to clearly identify the signals and clarify their respective functions, Claim 20, and thus Claim 21, comport with 35 USC 112 (second paragraph).

REJECTIONS UNDER 35 USC 102

Claims 1-3 and 7 are rejected under 35 USC 102(b) as anticipated by US Patent No. 5,703,807 to Smayling, et al. (Smayling). Applicants have reviewed the reference cited and respectfully assert it does not anticipate the embodiments of the present invention as recited in Claims 1-3, and 7 for the following rationale.

As Applicants understand the reference, Smayling teaches a circuit and method for generating erase and programming voltages for an EEPROM array. While Smayling teaches such a circuit and method, Applicant respectfully asserts that Smayling teaches that the programming voltage ramps up as shown in Figures 4 and 5 therein, which respectively depict a constant positive slope ramp up to a maximum value and a two stage, dual positive slope ramp up to a maximum value. Applicant respectfully asserts that ramping programming voltage up as taught by Smayling differs from, and in fact teaches away from the embodiment recited in Claim 1, as amended herein.

As amended herein, Claim 1 reads as follows:

1. A circuit for controlling the rise time of a signal, comprising:

a voltage multiplier which converts an input voltage to an output voltage greater than said input voltage;

a ramp generator coupled to said voltage multiplication circuit which controls said output voltage from said voltage multiplication circuit, wherein a ratio between a first capacitor of said ramp generator and a second capacitor of said ramp generator

determines said rise time of said signal, wherein said signal comprises a staircase ramp signal; and

a divide by N counter coupled to said ramp generator.

(underlining added herein for emphasis). As amended, Claim 1 recites that the signal comprises a staircase ramp, generated as a function of two capacitances. This allows the program voltage to be desensitized to factors such as process disparity, temperature change and difference, and power supply fluctuation, as explained in the specification from line 21 at page 10 to line 6 at page 11. Claims 2, 3, and 7 depend upon independent Claim 1.

Smayling does not teach this element of Claim 1, and in fact teaches away therefrom. Thus, Applicant respectfully asserts that Smayling does not anticipate or suggest Claims 1-3 and 7.

REJECTIONS UNDER 35 USC 103

Claims 3 and 9 are rejected under 35 USC 103(a) in view of Smayling. Claims 3 and 9 depend upon independent Claim 1, amended herein as discussed above. Claims 3 and 9 thus incorporate each and every element recited in Claim 1, including that the program voltage signal comprises a staircase ramp, generated as a function of two capacitances. As discussed above, this advantageously allows the program voltage to be desensitized to factors such as process disparity, temperature change and difference, and power supply fluctuation.

In contrast, Smayling teaches that the programming voltage ramps up as shown in its Figures 4 and 5. Smayling's Figure 4 and 5 respectively depict a constant positive slope ramp up to a maximum value and a two stage, dual positive

slope ramp up to a maximum value. Applicant respectfully asserts that ramping programming voltage up as taught by Smayling expressly teaches away from the embodiment recited in Claim 1, as amended herein. Thus, Applicant respectfully asserts that the reference also expressly teaches away from the embodiments recited in Claims 3 and 9. In as much as the reference expressly teaches away from these embodiments, Applicant respectfully asserts that, even in view of Smayling, Claims 3 and 9 are allowable under 35 USC 103(a).

CONCLUSION

By the rationale stated above, the Applicant respectfully asserts that the embodiments of the present invention as recited in Claims 14-21 comport with 35 USC 112 (second paragraph). By the rationale stated above, the Applicant also respectfully asserts that the embodiments of the present invention as recited in Claims 1-3 and 7 are allowable under 35 USC 102(b). Further, Applicant respectfully asserts that the embodiments of the present invention as recited in Claims 3 and 9 are allowable under 35 USC 103(a). The Applicant respectfully asserts therefore that Claims 1-3, 5, 7-12, and 14-21 are in condition for allowance.

Accordingly, Applicants respectfully request that the rejection of Claims 14-21 under 35 U.S.C. 112 (second paragraph), Claims 1-3 and 7 under 35 U.S.C. 102(b) and Claims 3 and 9 under 35 USC 103(a) be withdrawn and that Claims 1-3, 5, 7-12, and 14-21 be timely allowed.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: July 21, 2004

Lawrence R. Goerke
Reg. No. 45,927

WAGNER, MURABITO & HAO, LLP
Two North Market Street, Third Floor
San Jose, CA 95113

Tel.: (408) 938-9060
Fax: (408) 938-9069